DOCKET NO.: 105514 (NATI15-05514) **PATENT**
Customer No.: 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	FRANCISCO JAVIER GUERRERO MERCADO
Serial No.	:	10/619,169
Filed	:	July 14, 2003
For	:	LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY
Group	:	2816
Examiner	:	Tuan Thieu Lam

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief dated April 10, 2007, the Applicant is submitting a Substitute Appeal Brief. The Substitute Appeal Brief mainly provides additional information in the "Summary of the Claimed Subject Matter" section, namely a mapping of the independent claims to the disclosure.

If any outstanding issues remain or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

The Applicant has included the appropriate fee to cover the cost of a one (1) month extension of time. The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any additional extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: 6-6-2007

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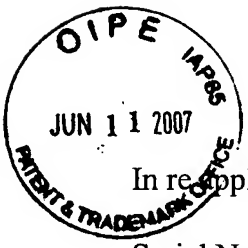

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APPELLANT'S SUBSTITUTE BRIEF ON APPEAL

This Substitute Brief is submitted on behalf of Appellant for the application identified above.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, NATIONAL SEMICONDUCTOR CORPORATION.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–20 are pending in the present application. Claims 7–8 and 15–20 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. Claims 1–3 and 10–11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,841,306 to *Lim*. Claims 1–3, 8–11 and 16–17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,323,695 to *Heinrich*. The rejection of pending claims 1–20 is appealed.

STATUS OF AMENDMENTS

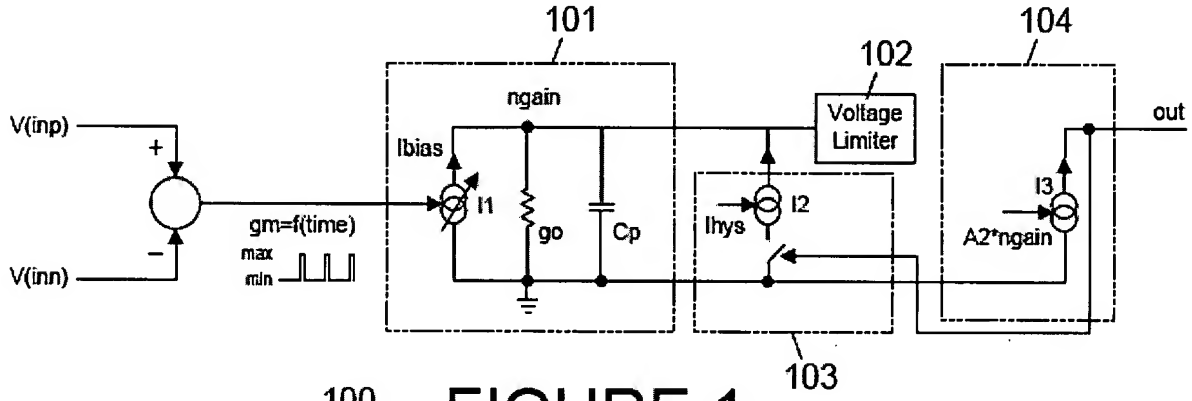
No amendment to the claims was filed following the final Office Action mailed September 13, 2005.

An amendment to the specification was submitted after final to cancel subject matter from the description and drawings. This amendment was refused entry by an Advisory Action mailed January 10, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

In general

The present invention generally relates to reduced propagation delay, low power comparators. In one embodiment, a comparator circuit 100 receives a pulsed transconductance gm produced from a differential input pair of signals V(inp) and V(inn) as an input at a first (input) gain stage 101.



100 FIGURE 1

Specification, ¶ [0016], Figure 1. The pulsed input (when pulsed rather than continuous) changes the bias current Ibias from the current source I1, changing the bias current of the whole comparator 100. Specification, ¶ [0016]. The output of the input gain stage 101 is connected to a voltage limiter 102 and a built-in hysteresis circuit 103 including a current source I2 driven by a hysteresis current signal Ihys. Specification, ¶ [0017]. The hysteresis current signal Ihys. is switched into and out of parallel connection with the input gain stage 101 based on the comparator's output voltage out. Specification, ¶ [0017]. A second (output) gain stage 104 is connected between the output of the

input gain stage 101 and an output signal out for the comparator circuit 100, and includes a current source I3 driven by a gain signal A2*ngain. Specification, ¶ [0017]. The second gain stage 104 changes gain A2*ngain based on the pulsed input, although in an optimized version the transition delay for the second gain stage 104 is negligible with respect to the transition delay of the first gain stage 101 such that the the gain of the second gain stage 104 may be treated as constant. Specification, ¶ [0018].

Comparator circuit 100 may be operated within one of a plurality of bias current values (e.g., between ibias/6 to 5*ibias). Specification, ¶ [0022]. When operated in a first, "low power" mode, the quiescent current of the amplifier (first or input gain stage 101) is driven with a constant bias current of ibias/6, so that comparator circuit 100 has low power consumption but a long propagation delay; when operated in a second, "fast comparator" mode, the quiescent current of the amplifier 101 is driven with a bias current of 5*ibias, such that comparator 100 has higher power consumption but a faster propagation delay. Specification, ¶¶ [0023]–[0025]. To reduce power consumption of the fast comparator mode, the bias current may be pulsed as described above, increasing power consumption by only about 50% over the slow comparator, continuous bias current mode despite the increase of bias current magnitude from ibias/6 to 5*ibias, and with an increase in propagation delay (e.g., from 30 μs to 0.8 μs, or more than 30 times faster). Specification, ¶¶ [0026]–[0028]. Thus the input bias current to the comparator may be either pulsed or continuous, depending on the operating mode, and may also be set to different levels or magnitudes for both operating modes.

Support for Independent Claims

Note that, per 37 C.F.R. § 41.37, only the independent claims are discussed in this section. The discussion of the claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.

Regarding Claim 1, an integrated circuit comparator (100) includes an input receiving an input signal representative of a difference between quantities to be compared. Specification, ¶ [0016], Page 8, Lines 14-18. The integrated circuit comparator (100) also includes an input gain stage (101) receiving the input signal and biased with a pulsed bias current. Specification, ¶ [0006], Page 4, Lines 3-11 and ¶ [0016], Page 8, Lines 14-20. The input gain stage (101) produces a gain based upon the input signal. Specification, ¶ [0002], Page 1, Lines 21-24.

Regarding Claim 9, a method of operating an integrated circuit comparator (100) includes receiving an input signal representative of a difference between quantities to be compared at an input for the comparator. Specification, ¶ [0016], Page 8, Lines 14-18. The method also includes transmitting the input signal from the input to an input gain stage (101) biased with a pulsed bias current. Specification, ¶ [0006], Page 4, Lines 3-11 and ¶ [0016], Page 8, Lines 14-20. The input gain stage produces a gain based upon the input signal. Specification, ¶ [0002], Page 1, Lines 21-24.

Regarding Claim 17, an integrated circuit includes a comparator (100) selectively operating in a first mode in which an input gain stage (101) of the comparator (100) is biased with a pulsed bias current and a second mode in which the input gain stage (101) is biased with a continuous bias

current. Specification, ¶ [0023], Page 10, Line 20 - Page 11, Line 5 and ¶¶ [0026]-[0028], Page 12, Line 3 - Page 13, Line 2.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 7–8 and 15–20 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

2. Claims 1–3 and 10–11 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Lim*.

3. Claims 1–3, 8–11 and 16–17 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Heinrich*.

ARGUMENT

1. The rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-195 (8th ed., rev. 3, August 2005). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *Id.* A patent need not teach, and preferably omits, what is well known in the art. *Id.* The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04 at 2100-197. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

a. The limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock."

The final rejection objects to the limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" in claims 7 and 15. However, it was well-known in the art at the time the application was filed that a global or "system" clock may be used to coordinately control various components or logical units within an integrated circuit. Such signals are understood to exist within

any system, and generally are NOT depicted in high level drawings (e.g., functional unit drawings, as opposed to circuit diagrams). Thus, those skilled in the art would not be confused by the absence of a expressly depicted system clock signal within a functional drawing of an integrated circuit.

The final rejection concedes that the absence of an expressly depicted system clock signal within a functional drawing of an integrated circuit would not confuse those skilled in the art. Paper No. 09102005, pages 6–7. However, the final rejection asserts that it is unclear as to how the pulsed bias current is generated at one edge of the system clock, and suggested that it would require undue experimentation for those skilled in the art to produce a pulse generator capable of generating a pulsed bias current that is a pulsed at one edge of a system clock. Applicant respectfully notes that such an assertion is wholly contradictory with the assertion in the Office Action that current Ib in U.S. Patent No. 5,841,306 to *Lin et al* comprises a pulsed bias current.

Moreover, at the time the application was filed, clock signals were well known to have rising and falling edges, and use of a clock edge to trigger an event or action ("edge-triggered") was also well-known. Paragraph [0029] of the application (copied below with emphasis added) clearly one structure for satisfying this claim limitation, a pulse generator (not depicted) producing a bias current pulse of 390 nano-second (ns) duration triggered on every falling edge of the 20 micro-second (μs) period and 50% duty cycle system clock clk and a comparator output is sampled on every rising edge of the system clock clk:

> [0029] *A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 ns bias current pulse.* Transistors within comparator 100 are sized

> for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before the falling edge of the system clock (clk) signal, where the system clock period is 20 μs and the clock duty cycle is 50%. *The pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge.*

The above-quoted paragraph describes how the pulsed bias current (in the exemplary embodiment) includes a pulse on the falling edge of the system clock and sampling a comparator output on the rising edge of the system clock. The above-quoted paragraph not only describes how the pulse bias current is produced (using a pulse generator triggered by the falling edge of the system clock to generate a 600 nano-Ampere (nA) pulse of 390 ns duration in an exemplary embodiment), but also provides specific requirements for the comparator (which influences the output of the comparator). For example, paragraph [0029] specifies for this exemplary embodiment that a pulsed generator be coupled to the comparator and produces a 390 ns bias current pulse. Transistors within the comparator are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs.

In addition, the assertion within the Office Action that those skilled in the art would be required unduly experiment in order to generate edge-triggered signals is wholly contradictory with the assertion in the Office Action that current Ic3 in *Heinrich* has the pulse shaped current recited in the claims.

The application as filed adequately enables generating a pulsed bias current, and triggering the pulse bias current on one edge of the system clock while sampling an output of the comparator

on the other edge. Accordingly, no undue experimentation would be required for those skilled in the art to implement such features as required by the claims.

b. **The limitations "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value," "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current," and "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current."**

The final rejection also objects to the limitations "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value" in claim 8, the limitation "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current" in claim 16, and the limitation "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current" in claim 17. Specifically, the final rejection contends that it is unclear as to how the circuit shown in Figures 4A and 4B enable operation in a first and second mode:

> Page 11, lines 6–25; page 12, lines 1–25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the circuit shown in figures 4A and 4B enable operatively in first and second modes** as called for in claim 8. That is, it is unclear as to how the comparator is selected to operate in a first mode in which the input gain stage is biased by a bias current with a defined first level value or when the comparator is selected to operate in a second mode the input gain stage is biased a bias current with a different second level value without undue experimentation.

Paper No. 09102005, page 3 (emphasis in original). Paragraph [0023] of the application as filed states:

> [0023] In an i_power_low_speed mode (or "low power comparator" configuration), the quiescent current of the amplifier (first gain stage 101) is driven with a constant bias current of ibias/6, so that comparator 100 has low power consumption but a long propagation delay slow_prop. In an i_power_high_speed mode (or "fast comparator" configuration), the quiescent current of the amplifier is driven with a constant bias current of 5*ibias, such that comparator 100 has higher power consumption but a faster propagation delay fast_prop.

The application clearly describes the implementation of different modes and different current levels for a functional unit. The exemplary embodiment in Figure 2A depicts the timing diagram of operation in a low speed mode, while Figures 2B and 2C depict the timing diagrams of operation in a high speed mode. Each mode is driven by different bias current values. For example, when the current in the first gain stage 101 is driven with a constant bias current of ibias/6, the comparator will generally operate in a low speed mode. On the other hand, when the current in the first gain stage 101 is driven with a constant bias current of 5* ibias, then the comparator will generally operate in a high speed mode. Applicant's Specification, ¶ [0023], pp. 10-11. The application thus adequately

enables selective operation of a comparator in a first mode and in a second mode. The fact that the feature is not ALSO enabled by the partial circuit diagrams of Figures 4A and 4B is irrelevant.

c. The limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal."

The final rejection further objects to the limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal" in claim 19. The Office Action states:

> Figure 1 shows "**an equivalent circuit**" of the actual present invention. The equivalent circuit shows a symbol of a variable current (ibias) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification use waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the current source being biased by the pulse of continuous bias current and controlled by the input current would correspond to the actual components of the actual comparator shown in figures 4A and 4B.**

Paper No. 09102005, pages 3–4 (emphasis in original). Figure 1 depicts, within the first (input) gain stage 101, a current source I1 producing bias current ibias and controlled by pulsed transconductance signal gm. These features are similar to the corresponding features of Figure 5 as filed (now Figure 4), illustrating known integrated circuit comparators. Moreover, the application as filed states:

> [0016] FIGURE 1 depicts an equivalent circuit diagram for a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. Comparator circuit 100 is formed within an integrated circuit device and includes a differential input pair V(inp) and V(inn) producing a pulsed transconductance gm received as an input by a first gain stage 101. The pulse input changes the bias current Ibias from the current source I1, changing the bias current of the whole comparator 100.
> [0017] The first gain stage 101 includes an output resistance go and output capacitance (including Miller capacitance) Cp in parallel with the current source I1.

> Connected to the output of the first gain stage 101 is a voltage limiter 102 and a built-in hysteresis circuit 103 including a current source I2 driven by a hysteresis current signal Ihys that is switched into and out of parallel connection with the first gain stage 101 at the output of the first gain stage 101 based on the comparator's output voltage out. Connected between the output of the first gain stage 101 (and to hysteresis circuit 103) is a second gain stage 104 including a current source I3 driven by a gain signal A2*ngain.

The structures depicted in the equivalent circuit diagram of Figure 1 may be readily implemented by those skilled in the art, such that no undue experimentation would be required for those skilled in the art to implement the features recited in claim 19.

2. The rejection of claims 1–3 and 10–11 under 35 U.S.C. § 102(e) as being anticipated by *Lim*.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8th ed. rev. 3 August 2005).

Independent claims 1 and 9 each recite an input gain stage biased with a pulsed bias current. Such a feature is not found in the cited reference. *Lim* teaches a bias control unit 10 controlling whether or not bias current is provided to comparator 20, providing bias current in an operating mode and not providing bias current during a power-saving mode as determined by the state of a mode control "trigger" input signal Vtri. However, *Lim* does not teach providing a pulsed bias current – that is, a current that is pulsed in accordance with a system clock – rather than a continuous bias current. Merely preventing the bias current from being supplied during periods when the comparator is not needed in order to reduce power consumption (as in the low power mode disclosed in the instant application) does not constitute provision of a "pulsed" bias current (one that is alternately on and then off during each clock cycle) rather than a continuous bias current.

The specification as filed teaches that the pulse bias current comprises a pulse on each falling edge of the system clock, a 390 ns pulse within a 20 μs system clock period in the exemplary embodiment. Because the specification as filed compels an interpretation of "pulsed bias current" as a bias current that is alternately on and then off during each clock cycle, the interpretation asserted in the final rejection – even if reasonable (which Appellants dispute) – cannot be accepted. *In re*

Johnston, 435 F.3d 1381, 1384 (Fed. Cir. 2006) (broader interpretations of claim limitations "must give way to the meaning imparted by the specification"), citing *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

The Office Action states:

> Regarding claims 1-3 and 10-11 as being anticipated by Lim (USP 5,841,306), applicant argues that Lim does not show input gain stage biased with a pulsed bias current as called for in claims 1-3 and 10-11 is no persuasive. Figure 5C of Lim clearly shows the bias current Ib as a pulse current biasing the input gain stage in figure 4. Therefore, the rejection is deemed proper.

Paper No. 09102005, page 8. However, as previously noted, a "pulsed" bias current as used in the specification is one that is pulsed (turn on and then turned off) during each cycle of the system clock:

> [0006] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide, for use in an integrated circuit comparator, ***a pulsed rather than continuous bias current applied, in at least a fast comparator configuration, to a current source within a comparator's input gain stage***. The transconductance current will then be pulsed rather than continuous. ***The pulse width of the bias current is small relative to the system clock***, but has a large current magnitude allowing the comparator to quickly respond to applied voltages. The end result is a fast comparator but without the large quiescent current associated with conventional fast comparators. A voltage limiter optimizes the ngain node voltage excursion. A built-in hysteresis circuit suppresses any spurious voltage spikes at the output node at every comparator's bias pulse. ***The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.***

Specification, ¶ [0006] (emphasis added). In the exemplary embodiment, the specification teaches that the bias pulses have a duration of 390 nanoseconds (0.39 microseconds) while the system clock period is 20 microseconds, for a bias current duty cycle of 1.95%. Specification, ¶¶ [0026]-[0027]. The specification thus makes clear that "pulsed" is used to indicate that the bias current is "on"

during only a portion of each clock cycle, as opposed to "continuous" bias current in which the bias current is on during the entire clock cycle, as depicted by the transconductance signal gm in Figure 1:

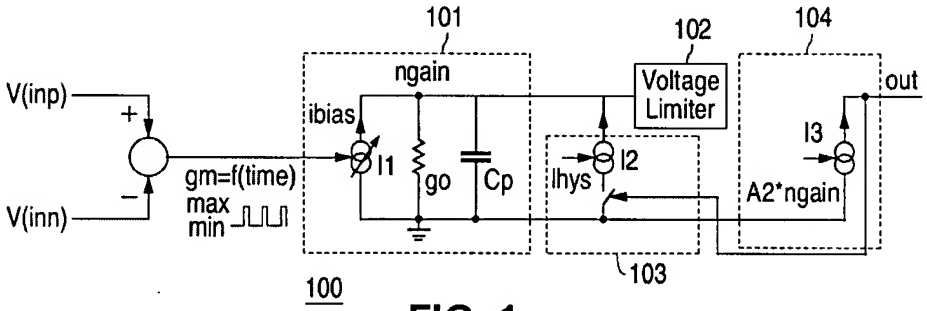


FIG. 1

By contrast, *Lim* depicts a current Ib that is turned on (by trigger signal Vtri depicted in Figure 5B) when the comparator is needed and turned off when the comparator is no longer needed (also by trigger signal Vtri depicted in Figure 5B):

FIG. 5B

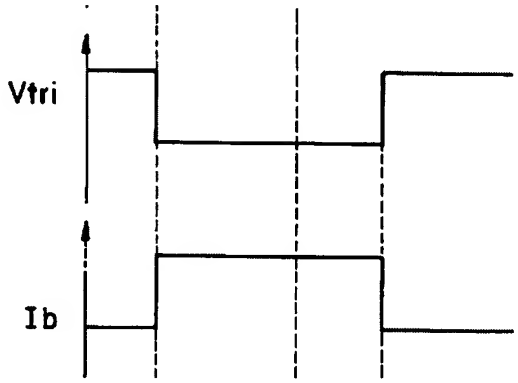


FIG. 5C

While the system clock is not depicted in *Lim* (as conventional), it is understood that the period during which current Ib is "on" encompasses multiple clock cycles. Nothing in *Lim* suggests that the period during which current Ib is "on" is less than (or even equal to) a single clock cycle.

Switching the comparator off when not needed as taught by *Lim* is analogous to the low power mode operation of the present invention, in which a continuous bias current is provided, but only when the comparator is "enabled":

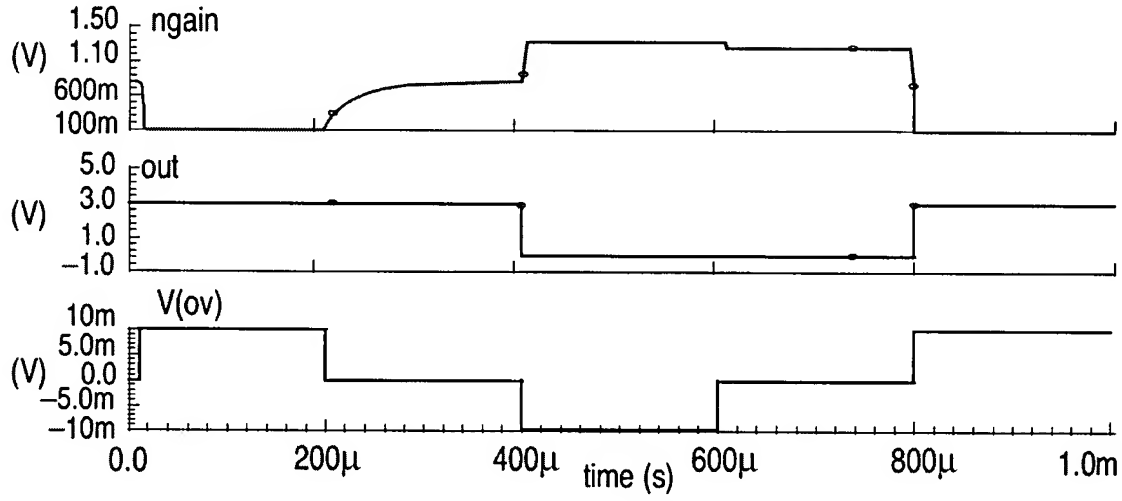


FIG. 2A

In the low power embodiment of the present invention, the comparator is effectively disabled (output voltage goes to zero) when the overdrive voltage V(ov) – the counterpart in the present invention to the trigger voltage Vtri in *Lim* – reaches a predetermined level. The comparator is similarly disabled during operation with a pulsed bias current:

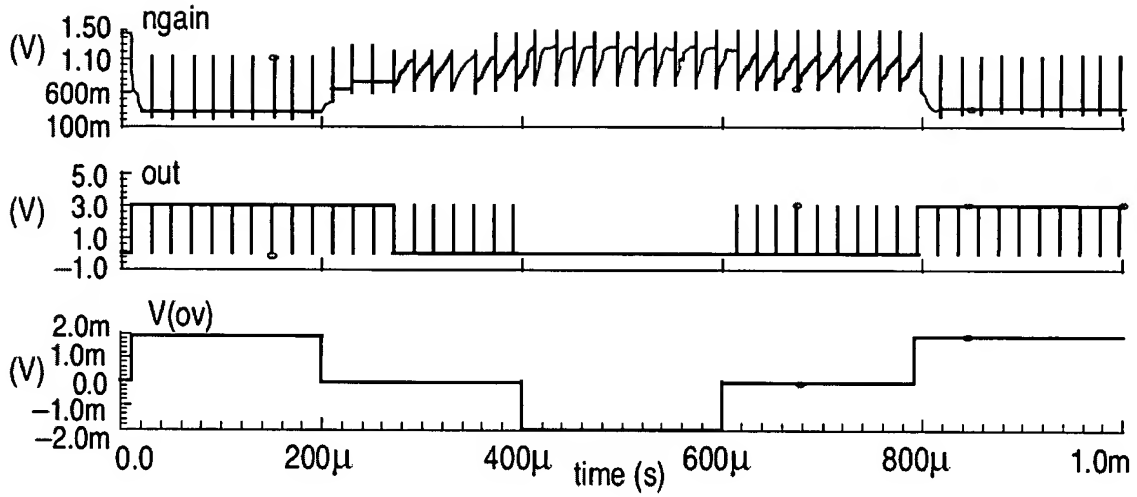


FIG. 2C

The use of a pulsed bias current while a comparator is operational is thus distinct from (and in addition to) disabling the comparator when not needed, as disclosed in both *Lim* and the specification. The current Ib "pulse" in *Lim* is thus NOT a "pulsed" bias current as that term is employed in the specification and claims of the present application, and *Lim* does not anticipate the pending claims.

Claims 2 and 10 each recite that the input signal is a current representative of transconductance of a differential pair of input transistors. Such a feature is not found in the cited reference. The current from the emitters of transistors Q8 and Q9 into terminal (b) of control circuit 10 in *Lim* merely determines whether the comparator 20 is on or off (for the power saving mode). The input signals to comparator 20 in *Lim* are (a) voltages Vth and Vref, not a current as recited in the claims, and (b) two separate voltages, not a single current as recited in the claims.

3. **The rejection of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102(e) as being anticipated by *Heinrich*.**

As noted above, independent claims 1 and 9 each recite an input gain stage biased with a pulsed bias current. Such a feature is not found in the cited reference. *Heinrich* teaches providing a continuous bias current Io at varying levels depending on an operating mode (i.e., whether the input signal is constant or varying):

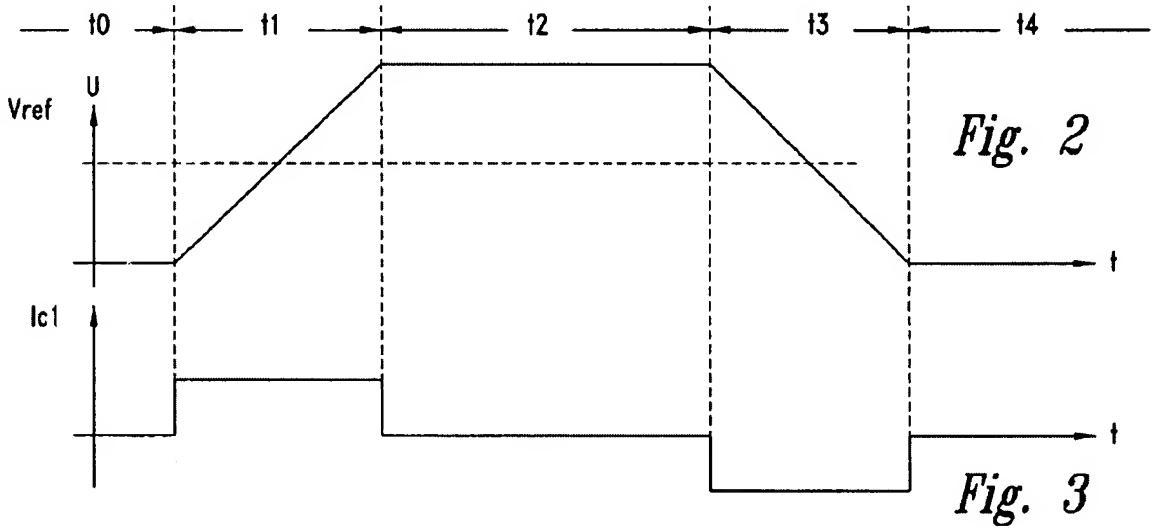


Fig. 2

Fig. 3

Heinrich does not even state that the bias current Io is ever turned off, but instead merely teaches that the magnitude of current Io varies between different levels (Io, Io+Ic1, or Io+Ic2). This is analogous to the provision of different magnitude (ibias/6 or 5*ibias) continuous bias currents as disclosed in the present invention, which also distinct from (and in addition to) providing a pulsed bias current. Merely altering levels for the bias current does not comprise pulsing the bias current as required by the claims. In that regard, the Office Action states:

> Regarding the rejection claims 1-3, 8-11 and 16-17 as being anticipated by Heinrich (USP 6,323,695), applicant argues that Heinrich does not show pulsed bias current as called for in claims 1-3, 8-11 and 16-17 is not persuasive. The current Ic1 in figure 3 having a pulse shape waveform anticipating the limitations called for in claims 1-3, 8-11 and 16-17. Therefore, the rejection is deemed proper.

Paper No. 09102005, page 9. However, the interpretation of the claim term "pulsed bias current" as encompassing any bias current that can be arbitrarily characterized as having the shape of a pulse is inconsistent with the specification, drawings and claims as filed, and is therefore arbitrary and capricious. Moreover the interpretation adopted by the Examiner has been disclaimed by the Applicant during prosecution.

As noted above, claims 2 and 10 each recite that the input signal is a current representative of transconductance of a differential pair of input transistors. Such a feature is not found in the cited reference. The transistors T1 and T2 in *Heinrich* are a differential amplifier comparing the input signal U to the reference voltage Vref to produce an output signal So, not an input gain stage:

> In a way known in the art, the comparator shown in FIG. 1 has a differential amplifier stage with two transistors T1 and T2. The gate terminal of said transistor T2 is connected with signal input Si of the comparator, which is supplied with an input signal U. A detail of an example of such an input signal U is shown in FIG. 2. The gate terminal of transistor T2 is connected with reference voltage source REF, which supplies reference voltage Vref to the gate terminal of T2.
>
> . . . .
>
> In the way likewise known in the art, low potential side current mirror Sp4 of the differential amplifier is constructed with, three current mirror branches. A connecting point between transistor T2 and current: mirror Sp4 forms output terminal So of the comparator.

Heinrich, column 3, lines 1–9 and 45–47. The inputs to the comparator formed by transistors T1 and T2 are voltages U and Vref, not a current as recited in the claims, and two voltages rather than a single current as recited in the claims.

Claims 16 and 17 each recite that the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current. Such a feature is not found in the cited reference. As noted above, *Heinrich* teaches that the bias current Io at node S is, continuously during a given period of operation, either Io, Io+Ic1 or Io+Ic2. Nowhere does *Heinrich* teach that the bias current Io is either continuous or pulsed. Even if the interpretation of *Heinrich* advanced in the final rejection is accepted (i.e., that the changes between levels constitutes a "pulsed" bias current), then *Heinrich* still fails to satisfy the limitation because no "continuous" bias current is also disclosed in *Heinrich*.

CONCLUSION

The subject matter of claims 7–8 and 15–20 is enabled by the specification as filed. Therefore, the rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph is improper. The cited references fail to disclose every limitation of the claimed invention. Therefore, the rejections of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102 are improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–20 in this application.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Original) An integrated circuit comparator comprising:

an input receiving an input signal representative of a difference between quantities to be compared; and

an input gain stage receiving the input signal and biased with a pulsed bias current, the input gain stage producing a gain based upon the input signal.

2. (Original) The integrated circuit comparator according to claim 1, wherein the input signal is a current representative of transconductance of a differential pair of input transistors.

3. (Original) The integrated circuit comparator according to claim 1, wherein the input gain stage further comprises a current source biased by the pulsed bias current and controlled by the input signal.

4. (Previously Presented) The integrated circuit comparator according to claim 1, further comprising:

a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

5. (Previously Presented) The integrated circuit comparator according to claim 4, further comprising:

an output gain stage coupled to the hysteresis circuit and having a gain varying with the bias change of the input gain stage.

6. (Original) The integrated circuit comparator according to claim 4, further comprising:

an output gain stage coupled to the hysteresis circuit and having a fixed gain and a propagation delay negligible with respect to a propagation delay of the input gain stage.

7. (Original) The integrated circuit comparator according to claim 1, wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock.

8. (Previously Presented) The integrated circuit comparator according to claim 1, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value.

9. (Original) A method of operating an integrated circuit comparator comprising:

receiving an input signal representative of a difference between quantities to be compared at an input for the comparator; and

transmitting the input signal from the input to an input gain stage biased with a pulsed bias current, the input gain stage producing a gain based upon the input signal.

10. (Original) The method according to claim 9, wherein the input signal is a current representative of transconductance of a differential pair of input transistors.

11. (Original) The method according to claim 9, wherein the input gain stage further comprises a current source biased by the pulsed bias current and controlled by the input signal.

12. (Previously Presented) The method according to claim 9, further comprising:

with an output signal from the input gain stage, driving a voltage limiter and a hysteresis circuit coupled to the output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

13. (Original) The method according to claim 12, further comprising:

varying a gain of an output gain stage coupled to the hysteresis circuit with the bias change of the input gain stage.

14. (Original) The method according to claim 12, further comprising:

fixing a gain of an output gain stage coupled to the hysteresis circuit and having a propagation delay negligible with respect to a propagation delay of the input gain stage.

15. (Original) The method according to claim 9, wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock.

16. (Original) The method according to claim 9, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current.

17. (Original) An integrated circuit comprising:

a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current.

18. (Original) The integrated circuit according to claim 17, wherein the input gain stage receives an input signal representative of a difference between quantities to be compared and produces a gain based upon a current for the input signal representative of transconductance of a differential pair of input transistors.

19. (Previously Presented) The integrated circuit according to claim 18, wherein the input gain stage further comprises a current source producing the pulsed or continuous bias current and controlled by the input signal.

20. (Previously Presented) The integrated circuit according to claim 19, further comprising:

a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.